Attorney Docket No.: 241014US2S DIV

Inventor: Koichi KOKUBUN PRELIMINARY AMENDMENT

IN THE CLAIMS

Please amend the claims as follows:

Claim 1-6 (Canceled)

Claim 7 (Original) A method of manufacturing a semiconductor device, comprising:

forming a trench in an SOI substrate, the trench extending from a major surface of

the SOI substrate and passing through a buried insulating film;

forming a first insulating film in the trench, a first insulating film with a depth to

reach an upper surface of the buried insulating film;

forming a second insulating film in a sidewall portion of the trench above the first

insulating film, the second insulating film made of a material different from that of the first

insulating film;

etching back the first insulating film to such a depth as to reach an upper surface of

the buried insulating film, using the second insulating film as a mask, and recessing the

buried insulating film exposed to the sidewall portion of the trench;

forming a semiconductor layer by epitaxial growth in a gap created by the recessed

buried insulating film; and

removing the first insulating film and the second insulating film and forming a trench

capacitor in the trench.

Claim 8 (Original) A method according to clam 7, further comprising forming a first

transistor in the SOI substrate, wherein the first transistor and the trench capacitor form a

DRAM memory cell.

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Claim 9 (Original) A method according to claim 7, further comprising forming a

second transistor in the SOI substrate, wherein the second transistor forms a logic circuit.

Claim 10 (Original) A method according to claim 8, further comprising forming a

second transistor in the SOI substrate, wherein the second transistor forms a logic circuit.

Clam 11 (Original) A method according to claim 10, wherein at least a part of a

manufacturing process of the transistor forming the DRAM memory cell is common to that

of the transistor forming the logic circuit.

Claim 12 (Original) A method according to claim 7, wherein the SOI substrate is

formed by bonding oxide film sides of two semiconductor substrates each having the oxide

film on one surface thereof.

Claim 13 (Original) A method of manufacturing a semiconductor device,

comprising:

forming a trench in an SOI substrate, the trench extending from a major surface of

the SOI substrate and passing through a buried insulating film;

forming a first insulating film in the trench, the first insulating film with a depth to

reach an upper surface of the buried insulating film;

forming a second insulating film in a sidewall portion of the trench above the first

insulating film, the second insulating film made of a material different from that of the first

insulating film;

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etching back the first insulating film to such a depth as to reach an upper surface of

the buried insulating film, using the second insulating film as a mask, and recessing the

buried insulating film exposed to the sidewall portion of the trench;

depositing a polysilicon layer on a major surface of the SOI substrate and in the

trench;

etching back the polysilicon layer by performing anisotropy etching to cause the

polysilicon layer to remain in a gap created by the recessed buried insulating film in the

trench; and

removing the first insulating film and a second insulating film and forming a trench

capacitor in the trench.

Claim 14 (Original) A method according to claim 13, further comprising forming a

first transistor in the SOI substrate, wherein the first transistor and the trench capacitor form

a DRAM memory cell.

Claim 15 (Original) A method according to claim 13, further comprising forming a

second transistor in the SOI substrate, wherein the second transistor forms a logic circuit.

Claim 16 (Original) A method according to claim 14, further comprising forming a

second transistor in the SOI substrate, wherein the second transistor forms a logic circuit.

Claim 17 (Original) A method according to claim 16, wherein at least a part of a

manufacturing process of the transistor forming the DRAM memory cell is common to that

of the transistor forming the logic circuit.

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Claim 18 (Original) A method according to claim 13, wherein the SOI substrate is formed by bonding oxide film sides of two semiconductor substrates each having the oxide film on one surface thereof.